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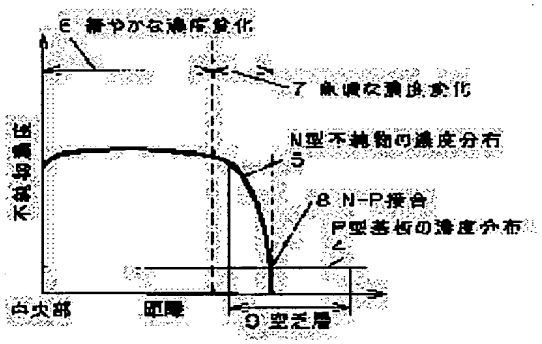
(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : SHIBATA YOSHIYUKI
HIRASE JUNJI
HORI TAKASHI

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To obtain a semiconductor device in which the leakage current of a P-N junction formed between an impurity region and a semiconductor substrate and its change amount are reduced while the semiconductor device is being made fine when the potential of the substrate or the impurity region is changed regarding the impurity region which is formed inside the substrate and whose conductivity type is opposite to that of the substrate.
CONSTITUTION: In a semiconductor device provided with an N-type impurity region, the state of an impurity concentration distribution 5 in the N-type impurity region inside a P-type substrate is set at a gentle concentration gradient 6 at the inside of the impurity region, the state is set at a steep concentration gradient 7 near an N-P junction 8 which is formed between a concentration distribution 4 for the P-type substrate and the N-type impurity concentration distribution 5, and the leakage current of a P-N junction and its change amount can be reduced.



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CLAIMS

[Claim(s)]

[Claim 1] The semiconductor device which it was concentration distribution loose inside the field which said semi-conductor substrate and P-N junction were ****(ed), and concentration distribution changed steeply near [said] P-N junction, and was separated from said P-N junction to the position in a 1 conductivity-type semi-conductor substrate, and also was equipped with the impurity range of a conductivity type.

[Claim 2] The manufacture approach of the semiconductor device equipped with the process which introduces the impurity of other conductivity types into the position in a 1 conductivity-type semi-conductor substrate by the ion implantation, and forms the impurity range of other conductivity types, the process which introduces a fluorine into the position of said impurity range by the ion implantation, and the process which heat-treats to said substrate.

[Claim 3] The manufacture approach of the semiconductor device according to claim 2 characterized by using the impregnation mask used when carrying out the ion implantation of the impurity of other conductivity types as a mask when carrying out the ion implantation of the fluorine.

[Claim 4] The manufacture approach of the semiconductor device according to claim 2 or 3 characterized by performing the ion implantation of a fluorine by the large inclination to a substrate.

[Claim 5] It is [a component isolation region and] MOS to a 1 conductivity type semi-conductor substrate front face . Semiconductor device with which concentration distribution was equipped with the source drain field which changes steeply near the junction of the desired location form between substrates while it consisted of a gate electrode formed in the part used as a mold transistor field , and an impurity of other conductivity types and had concentration distribution loose inside .

[Claim 6] The manufacture approach of the semiconductor device equipped with the process which forms the part used as a component isolation region and a MOS-transistor field in a 1 conductivity-type semi-conductor substrate front face, the process which forms a gate electrode in the part used as

said MOS-transistor field, the process which introduces the impurity of other conductivity types by the ion implantation, and forms a source drain field, the process which introduce a fluorine into the position of said source drain field by the ion implantation, and the process which heat-treat to said substrate.

[Claim 7] The manufacture approach of the semiconductor device according to claim 6 characterized by using the same thing for the ion-implantation mask for source drain field formation, and the mask of the ion implantation of a fluorine.

[Claim 8] The manufacture approach of the semiconductor device according to claim 6 or 7 characterized by performing the ion implantation of a fluorine by the large inclination to a substrate.

[Claim 9] The semiconductor device equipped with the impurity range of concentration thinner than said source / drain field with the conductivity type besides a wrap for all or some of the gate electrode formed in the 1 conductivity-type semi-conductor substrate front face at the part used as a component isolation region and a MOS transistor field, the source / drain field which consists of an impurity of said other conductivity types, and said source / drain fields.

[Claim 10] The process which forms the part used as a component isolation region and a MOS transistor field in a 1 conductivity-type semi-conductor substrate front face, The process which forms a gate electrode in the part used as said MOS transistor field, The process which introduces the impurity of other conductivity types by the ion implantation, and forms the impurity range of thin concentration, The manufacture approach of the semiconductor device equipped with the process which introduces the impurity of said other conductivity types by the ion implantation, and forms the source / drain field, the process which introduces a fluorine into the position of the impurity range of said thin concentration by the ion implantation, and the process which heat-treats to said substrate.

[Claim 11] The manufacture approach of the semiconductor device according to claim 10 characterized by using the same thing for the thin ion-implantation mask for impurity range formation of concentration, and the mask of the ion implantation of a fluorine.

[Claim 12] The manufacture approach of the semiconductor device according to claim 10 or 11 characterized by performing the ion implantation of a fluorine by the large inclination to a substrate.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a semiconductor device and its manufacture approach.

[0002]

[Description of the Prior Art] Conventionally, installation of the impurity to the inside of a semi-conductor substrate and formation of an impurity range have an approach by the thermal diffusion from the substrate front face of heat-treating by placing into the ambient atmosphere containing the impurity of a request of a substrate, and a method of introducing a desired impurity into a substrate with ion-implantation, and adding heat treatment for activation of an impurity.

[0003] The distribution condition of the impurity within the substrate when using these approaches is explained using drawing 8 . An axis of ordinate shows high impurity concentration, and an axis of abscissa shows distance. First, in installation by thermal diffusion, an impurity invades from a substrate front face, and that impurity is diffused during this heat treatment. It decreases gently-sloping as for this reason the distribution 103 of an impurity becomes high concentration and becomes deep from a front face after that on a front face. When an ion implantation and heat treatment are used, the distribution condition of an impurity serves as the so-called Gaussian distribution about one ion implantation, and acceleration energy determines the peak location of concentration. Moreover, the distribution at the time of performing acceleration energy various with the same impurity and the ion implantation of a dose will be in the distribution condition which the distribution about each impregnation overlapped and was added in each location.

[0004] By the way, drawing is coming improvement in a degree of integration, and improvement in the engine performance by the semiconductor device by performing much more detailed-ization. As one of the means which performs detailed-ization, there is control of diffusion of the conductivity-type impurity introduced into the semi-conductor substrate. This is controlling the breadth of the impurity to a horizontal or a perpendicular direction to a substrate front face, and is an approach aiming at each components made detailed making it operate, without connecting too hastily electrically physical again. It is the approach of making the impregnation energy low and specifically making it shallow, if it is ion-implantation about installation of an impurity when forming an impurity range near a substrate front face like the

approach of shortening time amount, for example, the source/drain of a MOS transistor, or it low-temperature-izes temperature of a heat treatment process etc.

[0005] MOS mold structure is explained using drawing 9 . Generally a MOS transistor consists of isolation 121, a gate electrode 122, and the source / drain field 128. For example, the LDD (Lightly Doped Drain) field 125 formation which makes others thinly the source / drain concentration directly under the gate for securing dependability with the structure of a MOS transistor, For example, the P.T.S. (punch through stop) field 126 formation only whose position in a substrate makes substrate concentration deep for short-channel-effect control, For example, the C.S. (channel stop) field 124 formation which makes deep substrate concentration directly under a component isolation region for the improvement in a separation proof pressure is taken in, and improvement in the engine performance is achieved. Moreover, formation of these impurity ranges is performed by the thermal diffusion of the impurity of a top description poor request, or the combination of an ion implantation and heat treatment.

[0006]

[Problem(s) to be Solved by the Invention] however, by the approach of forming an impurity range in the combination of the above thermal diffusion and ion implantations, and heat treatment When it explains using drawing 8 , the distribution condition of an impurity Have a high-concentration peak location in the interior of a field, and become steep [distribution of concentration] from the location immediately before and behind that. That is, although it is shallow, it becomes the steep distribution 104, or even if the distribution condition inside a field is loose, an impurity is spread considerably, and spreads in a horizontal / vertical both directions, that is, will become the loose but deep distribution 105.

[0007] Although P-N junction 111 is formed between an impurity range and a substrate at this time, the distribution condition of an impurity has a high-concentration peak in the interior of an impurity range, when it is distribution steep from this peak location to a tail location, if the potential of an impurity range changes and depletion-layer width of face changes in connection with this, since concentration distribution of an impurity range is steep, the variation of junction leakage current will also become rapid and the problem will change a lot will also produce substrate potential. Moreover, since the concentration of an impurity also becomes high, the problem that the power consumption at the time of junction leakage current itself increasing and constituting a circuit will increase arises.

[0008] Moreover, in the case where a formation process is made in simple, in order for the distribution condition inside an impurity range to make it loose, it is necessary to fully diffuse the impurity introduced by the ion implantation by heat treatment. In this case, since an impurity range spreads, the problem that it becomes difficult to achieve detailed-ization arises.

[0009] Distribution inside an impurity range is gently carried out to others, and there are level and an approach shown in drawing 8 (b) as approach which is not diffused perpendicularly about an impurity range. namely, the ion implantation of impurity installation -- acceleration energy -- gradual -- changing -- many times -- 106 -- carrying out -- heat treatment of activation -- low temperature -- and a short time -- ****** -- ** By this approach, it will not be in the distribution condition which produces the above problems. However, it is necessary to change acceleration energy and to carry out the ion implantation for impurity installation many times, and there is a problem that the increase in cost by the increment in a process will arise, by this approach.

[0010] Therefore, the object of this invention is between the impurity range which formed [a substrate inner-drainage common and] the impurity range in the substrate, being perpendicular, and not extending but attaining detailed-ization, and a substrate. P-N It is in offering the semiconductor device which controls the abrupt change of junction leakage current and increment which are generated about junction when changing the potential of an impurity or a substrate, and its manufacture approach.

[0011]

[Means for Solving the Problem] A semiconductor device according to claim 1 offers the semiconductor device which controls the abrupt change of junction leakage current and increment which are generated when changing the potential of an impurity or a substrate in view of the above-mentioned trouble about the P-N junction between the impurity range which formed [a substrate inner-drainage common and] the impurity range in the substrate, being perpendicular, and not extending but attaining detailed-ization, and a substrate. In the field which said semi-conductor substrate and P-N junction were formed in the position in a 1 conductivity-type semi-conductor substrate, and concentration distribution changed steeply near [said] P-N junction as a configuration for it, and was separated from said P-N junction, it is loose concentration distribution, and also is characterized by the structure of having the impurity range of a conductivity type.

[0012] The manufacture approach of the

semiconductor device claims 2 and 3 and four publications offers the manufacture approach of the semiconductor device which controls the abrupt change of junction leakage current and increment which are generated when changing the potential of an impurity or a substrate in view of the above-mentioned trouble about the P-N junction between the impurity range which formed [a substrate inner-drainage common and] the impurity range in the substrate, being perpendicular, and not extending but attaining detailed-ization, and a substrate. As a configuration for it, the impurity of other conductivity types is introduced into the position in a 1 conductivity-type semi-conductor substrate by the ion implantation, and it is characterized by having the process which forms the impurity range of said other conductivity types, the process which introduces a fluorine into the position of said impurity range by the ion implantation, and the process which heat-treats to said substrate.

[0013] A semiconductor device according to claim 5 offers the semiconductor device which controls the abrupt change of junction leakage current and increment which are generated when changing the potential of an impurity or a substrate in view of the above-mentioned trouble about the P-N junction between the source / drain field which formed [a substrate inner-drainage common and] the source / drain field of a MOS transistor in the substrate, being perpendicular, and not extending but attaining detailed-ization, and a substrate. concentration distribution be characterize by have the source drain field which change steeply near the junction form between the substrates of a desired location , consist of a gate electrode formed in the 1 conductivity type semi-conductor substrate front face as a configuration for it at the part used as a component isolation region and a MOS transistor field , and an impurity of other conductivity types , and have concentration distribution loose inside .

[0014] The manufacture approach of the semiconductor device claims 6 and 7 and eight publications offers the manufacture approach of the semiconductor device which controls the abrupt change of junction leakage current and the increment which are generated when changing the potential of an impurity or a substrate in view of the above-mentioned trouble about the P-N junction between the source / drain field which formed [a substrate inner-drainage common and] the source / drain field of a MOS transistor in the substrate, being perpendicular, and not extending but attaining detailed-ization, and a substrate. The process which forms the part used as a component isolation region and a MOS transistor field in a 1 conductivity-type semi-conductor

substrate front face as a configuration for it, Said MOS The process which forms gate dielectric film in the part used as a mold transistor field, The impurity of other conductivity types is introduced by the ion implantation, and it is characterized by having the process which forms a source drain field, the process which introduces a fluorine into the position of said source drain field by the ion implantation by using a resist as a mask, and the process which heat-treats to said substrate.

[0015] A semiconductor device according to claim 9 offers the semiconductor device which controls the abrupt change of junction leakage current and increment which are generated when changing the potential of an impurity or a substrate in view of the above-mentioned trouble about the P-N junction between the source / drain field which formed [a substrate inner-drainage common and] the LDD field of a MOS transistor in the substrate, being perpendicular, and not extending but attaining detailed-ization, and a substrate. It is characterized by having the gate electrode formed in the 1 conductivity-type semi-conductor substrate front face as a configuration for it at the part used as a component isolation region and a MOS transistor field, said semi-conductor substrate and LDD field of an another side conductivity type, and the source / drain field which consists of an impurity of other conductivity types.

[0016] The manufacture approach of the semiconductor device claims 10 and 11 and 12 publications offers the manufacture approach of the semiconductor device which controls the abrupt change of junction leakage current and increment which are generated when changing the potential of an impurity or a substrate in view of the above-mentioned trouble about the P-N junction between the source / drain field which formed [a substrate inner-drainage common and] the LDD field of a MOS transistor in the substrate, being perpendicular, and not extending but attaining detailed-ization, and a substrate. The process which forms the part used as a component isolation region and a MOS transistor field in a 1 conductivity-type semi-conductor substrate front face as a configuration for it, Said MOS The process which forms gate dielectric film in the part used as a mold transistor field, The process which introduces the impurity of other conductivity types by the ion implantation, and forms a LDD field, The impurity of said other conductivity types is introduced by the ion implantation, and it is characterized by having the process which forms the source / drain field, the process which introduces a fluorine into the position of the field which is said comparatively thin high impurity concentration by the ion

implantation, and the process which heat-treats to said substrate.

[0017]

[Function] P-N between the impurity range formed in the substrate, being level and perpendicular, and not extending the impurity range formed in the substrate or the source / drain field of a MOS transistor, and a LDD field, but attaining detailed-ization with the semiconductor device concerning claims 1, 5, and 9, and a substrate It becomes possible to control the abrupt change of junction leakage current and increment which are generated about junction when changing the potential of an impurity or a substrate.

[0018] The impurity range formed in the substrate by the manufacture approach of the semiconductor device concerning claims 2, 3, 4, 6, 7, 8, 10, 11, and 12 Or, being level and perpendicular, and not extending the source / drain field, and the LDD field of a MOS transistor, but attaining detailed-ization It becomes possible to control the abrupt change of junction leakage current and increment which are generated about the P-N junction between the impurity range formed in the substrate, and a substrate when changing the potential of an impurity or a substrate.

[0019]

[Example] Below, as one example of a semiconductor device according to claim 1, although detailed-ization is attained in the case of the N type impurity range formed in the P type substrate, it explains, referring to a drawing about the equipment which can reduce the leakage current of the P-N junction formed between a substrate and an impurity range, and its variation.

[0020] Drawing 1 is impurity atom concentration profile drawing for the explanation of operation in the example of this invention. By drawing 1 , when an axis of abscissa is used into distance and the zero of high impurity concentration and an axis of abscissa is used as the center section of the impurity range for an axis of ordinate about the concentration of the N type impurity formed in the P type substrate, the N-P junction 8 formed between the field of the loose concentration change 6, the field of the steep concentration change 7 and an N type impurity range, and a P type substrate is shown in the impurity distribution 4 of a P type substrate, the concentration distribution 5 of an N type impurity, and the concentration distribution 5 of an N type impurity. However, the N-P junction 8 shall be located in the concentration change 7 steep about an N type impurity range in this case.

[0021] Generally, if the P type of P-N junction or which potential of an N type field is changed, the depletion-layer width of face formed by P-N junction will change, and a junction current will flow.

If the potential of for example, an N type impurity range changes in the forward direction by taking this configuration, the depletion-layer width of face 9 of N-P junction will spread, but when a depletion-layer field arrives at concentration change 6 loose field, and concentration change becomes loose here, the augend of junction leakage current can also be reduced. The power consumption at the time of being able to reduce the absolute value of the leakage current from a joint itself for this reason, for example, forming a circuit can also be reduced.

[0022] Moreover, since the concentration change near the joint is steep, it can also attain detailed-ization of a component, without extending an impurity range.

[0023] As mentioned above, according to this example, although detailed-ization of a component is attained, the increment in the leakage current produced in the joint of a substrate and an impurity range and its variation can be controlled.

[0024] Below, as claims 2 and 3 and one example of the manufacture approach of a semiconductor device given in four, although detailed-ization is attained when an N type impurity range is formed in a P type substrate, it explains, referring to a drawing about the manufacture approach that the leakage current of the P-N junction formed between a substrate and an impurity range and its variation can be reduced.

[0025] Drawing 2 is the process sectional view of the example of this invention. Moreover, drawing 3 is impurity atom concentration profile drawing for the explanation of operation in this example.

[0026] drawing 2 (a) **** -- the ion-implantation mask 22 is used for the P type silicon substrate 21, for example, the ion implantation 23 of an N type impurity is performed on conditions, such as P, 30KeV, and 5E15 atoms/cm2, and the N type impurity range 24 is formed.

[0027] drawing 2 (b) -- the impregnation mask 25 -- using -- the ion implantation 26 of a fluorine -- for example, 35KeV(s) and 2E15 atoms/cm2 ** -- it carries out on the said conditions and (F) fluorine field 27 is formed in the pars basilaris ossis occipitalis of the N type impurity range 24. It heat-treats to a substrate 21 after that, and an N type impurity is activated.

[0028] Drawing 3 shows the N type impurity at the time of performing the above-mentioned heat treatment, and concentration distribution of F. An axis of ordinate expresses high impurity concentration, and an axis of abscissa expresses distance. In drawing 3 (a), the concentration distribution 31 of F immediately after an ion implantation to which the peak location 30 of concentration distribution of F crosses the peak location 32 of concentration distribution of an N type impurity to the concentration distribution 29

immediately after introducing an N type impurity into a P type substrate by the ion implantation is set up. It heat-treats in the state of this distribution.

[0029] It compares with the distribution 34 after heat treatment in case the concentration distribution 33 of after heat treatment and an N type impurity does not perform the conventional fluorine impregnation in drawing 3 (b), and is a fluorine. Although it has a loose change inside an N type impurity range under the effect of the diffusion depressor effect of (F), it changes steeply in the location distant from the peak.

[0030] At this time, since diffusion in heat treatment of an impurity range is controlled, detailed-ization of a component can be attained. In addition, without the leakage current of a joint increasing for impurity part [of N type loose even when the potential of an impurity range changes since it changed steeply near P-N junction with a substrate, although the distribution condition of an N type impurity changed gently inside the field, and the depletion-layer width of face of a joint spreads] blanket-like voice, since the variation is also loose again, the substrate potential itself does not change a lot. For the reason, the stable good semiconductor device can be formed.

[0031] In addition, as shown in drawing 2 (c) instead of the process shown in drawing 2 (b), fluorine impregnation may be performed using the mask 22 for ion implantations of the impurity of N type, and simplification of a process can be attained. At this time, the field 28 of a fluorine can be formed in the location of not only a pars basilaris ossis occipitalis but arbitration to the N type impurity range 24 by performing fluorine impregnation by the large inclination theta.

[0032] As mentioned above, according to this example, although detailed-ization of a component is attained, the increment in the leakage current produced in the joint of a substrate and an impurity range and its variation can be controlled.

[0033] Although detailed-ization is attained about the MOS transistor formed in the P type substrate as one example of a semiconductor device according to claim 5 below, it explains referring to a drawing about the equipment which can reduce the leakage current of the P-N junction formed between a substrate and an impurity range, and its variation. Drawing 4 is the sectional view of the semiconductor device at the time of applying this invention to a MOS transistor.

[0034] drawing 4 (a) **** -- in the MOS transistor which consists of the gate electrode 41, isolation 49, and N type the source / impurity range for drains 45, inside a field, make concentration part blanket-like voice of the source / N type impurity range 45 for drains into the

loose concentration change field 42, and let it be the rapid concentration change field 43 near the junction to a field pars basilaris ossis occipitalis and a substrate.

[0035] If the potential of the source / N type impurity range 45 for drains changes for example, in the forward direction by taking this configuration, the depletion-layer width of face of the N-P junction 44 will spread, but when a depletion-layer field arrives at concentration change 43 loose field, and concentration change becomes loose here, the augend of junction leakage current can also be reduced. Since the variation is loose, substrate potential does not change a lot. Moreover, the power consumption at the time of being able to reduce the absolute value of the leakage current from a joint itself, for example, forming a circuit can also be reduced. Since the concentration change near the joint is still steeper, it is also possible to attain detailed-ization of a component.

[0036] In drawing 4 (b), by make impurity distribution of the gate electrode direct bottom and the isolation direct bottom into the rapid concentration change field 2 (43b) and the rapid concentration change field 1 (43a) about the source / N type impurity range 45 for drains of a MOS transistor, the single channel effect which be the basic property of a transistor raise control or a separation property, and while attain detailed-ization, the increment in junction leakage current and its variation can be reduce.

[0037] As mentioned above, according to this example, although detailed-ization of a component is attained, the increment in the leakage current produced in the joint of a substrate and an impurity range and its variation can be controlled.

[0038] Although detailed-ization is attained about the case where a MOS transistor is formed in a P type substrate below as claims 6 and 7 and manufacture approach 1 example of a semiconductor device given in eight, it explains referring to a drawing about the manufacture approach that the leakage current of the P-N junction formed between a substrate and an impurity range and its variation can be reduced. Drawing 5 is a process sectional view at the time of applying this invention to the manufacture approach of a MOS transistor.

[0039] In drawing 5 (a), in forming the MOS transistor which becomes the P type substrate 21 from the gate electrode 41 and isolation 49, the source / N type impurity 51 for drains is introduced by the ion implantation using the impregnation mask 22, and the source / N type impurity range 45 for drains is formed.

[0040] In drawing 5 (b), a fluorine (F) is introduced by the ion implantation using the impregnation mask 25, and they are the source/object for drains. The fluorine (F) field 53 is formed in the pars basilaris

ossis occipitalis of the N type impurity range 45. Heat treatment is added to a substrate 21 after that.

[0041] They are the source/object for drains by performing the above-mentioned process in drawing 5 (c). Inside a field, make concentration part blanket-like voice of the N type impurity range 45 into the loose concentration change field 54, and let it be the rapid concentration change field 56 near the junction to a field pars basilaris ossis occipitalis and a substrate.

[0042] If the potential of the source / N type impurity range 45 for drains changes for example, in the forward direction by taking this configuration, the depletion-layer width of face of the N-P junction 56 will spread, but when a depletion-layer field arrives at concentration change 54 loose field, and concentration change becomes loose here, the augend of junction leakage current can also be reduced. Since the variation is loose, substrate potential does not change a lot. Moreover, the power consumption at the time of being able to reduce the absolute value of the leakage current from a joint itself, for example, forming a circuit can also be reduced. Since the concentration change near the joint is still steeper, it is also possible to attain detailed-ization of a component.

[0043] In addition, as shown in drawing 5 (d) instead of the process shown in drawing 5 (c), fluorine impregnation may be performed using the mask 22 for ion implantations of the impurity of N type, and simplification of a process can be attained. At this time, the field 58 of a fluorine can be formed in the location of arbitration called the field of for example, not only a pars basilaris ossis occipitalis but the gate electrode direct bottom, or the isolation direct bottom to the N type impurity range 45 by performing fluorine impregnation by the large inclination theta. While the single channel effect which is the basic property of a transistor raises control or a separation property and attaining detailed-ization, without this increasing a process, the increment in junction leakage current and its variation can be reduced.

[0044] As mentioned above, according to this example, although detailed-ization of a component is attained, the increment in the leakage current produced in the joint of a substrate and an impurity range and its variation can be controlled.

[0045] Below, as one example of a semiconductor device according to claim 9, although detailed-ization is attained about the MOS transistor formed in the P type substrate, it explains, referring to a drawing about the equipment which can reduce the leakage current of the P-N junction formed between a substrate and an impurity range, and its variation. Drawing 6 is the sectional view of a semiconductor device at the time of applying this invention to the MOS

transistor which has LDD structure.

[0046] In the MOS transistor which consists of the gate electrode 41, isolation 49, a LDD field 81, and N type the source / impurity range for drains 82, inside a field, make concentration part blanket-like voice of the LDD field 81 into the loose concentration change field 83, and let it be the rapid concentration change field 84 near the junction to a field and a substrate in drawing 6 .

[0047] If the potential of the LDD field 81 changes for example, in the forward direction by taking this configuration, the depletion-layer width of face of N-P junction will spread, but when a depletion-layer field arrives at concentration change 83 loose field, and concentration change becomes loose here, the augend of junction leakage current can also be reduced. Since the variation is loose, substrate potential does not change a lot. Moreover, the power consumption at the time of being able to reduce the absolute value of the leakage current from a joint itself, for example, forming a circuit can also be reduced. Since the concentration change near the joint is still steeper, it is also possible to attain detailed-ization of a component.

[0048] As mentioned above, according to this example, although detailed-ization of a component is attained, the increment in the leakage current produced in the joint of a substrate and an impurity range and its variation can be controlled.

[0049] Below, as claims 10 and 11 and one example of the manufacture approach of a semiconductor device given in 12, although detailed-ization is attained about the case where a MOS transistor is formed in a P type substrate, it explains, referring to a drawing about the manufacture approach that the leakage current of the P-N junction formed between a substrate and an impurity range and its variation can be reduced. Drawing 7 is a process sectional view at the time of applying this invention to the manufacture approach of the MOS transistor which has LDD structure.

[0050] In forming the MOS transistor which becomes the P type substrate 21 from the gate electrode 41 and isolation 49 in drawing 7 (a), the N type impurity 61 for LDD is introduced by the ion implantation using the impregnation mask 63, and it is an object for LDD. The N type impurity range 62 is formed.

[0051] In drawing 7 (b), a fluorine (F) is introduced by the ion implantation using the impregnation mask 25, and the fluorine (F) field 53 is formed in the pars basilaris ossis occipitalis of the N type impurity range 62 for LDD. Heat treatment is added to a substrate 21 after that.

[0052] In drawing 7 (c), a sidewall 64 is formed to the gate electrode 41, an ion implantation performs installation 68 of the deep N type impurity the source / for drains by using a gate electrode and the

impregnation mask 22 as a mask after that, and the source / drain field 65 is formed so that it may lap with some or all in the N type impurity range 62 for LDD. Heat treatment is added to a substrate 21 after that.

[0053] If the potential of the N type impurity range 62 for LDD changes for example, in the forward direction by taking this configuration, the depletion-layer width of face of N-P junction will spread, but when a depletion-layer field arrives at a loose concentration change field, and concentration change becomes loose here, the augend of junction leakage current can also be reduced. Since the variation is loose, substrate potential does not change a lot. Moreover, the power consumption at the time of being able to reduce the absolute value of the leakage current from a joint itself, for example, forming a circuit can also be reduced. Since the concentration change near the joint is still steeper, it is also possible to attain detailed-ization of a component.

[0054] In addition, fluorine impregnation may be performed using the mask 22 for ion implantations of the impurity of the thin N type for LDD shown in drawing 7 (d) instead of the process shown in drawing 7 (c), and simplification of a process can be attained. Moreover, the field 67 of a fluorine can be formed in the location of arbitration called the field of for example, not only a pars basilaris ossis occipitalis but the gate electrode direct bottom, or the isolation direct bottom to the N type impurity range 62 for LDD by performing fluorine impregnation 66 by the large inclination theta at this time. While the single channel effect which is the basic property of a transistor raises control or a separation property and attaining detailed-ization, without this increasing a process, the increment in junction leakage current and its variation can be reduced.

[0055] As mentioned above, according to this example, although detailed-ization of a component is attained, the increment in the leakage current produced in the joint of a substrate and an impurity range and its variation can be controlled.

[0056] In addition, the same effectiveness is acquired when the impurity range of P type, the source / drain field, and a LDD field are formed in an N type substrate in the above-mentioned example.

[0057]

[Effect of the Invention] The impurity range which formed this invention in the substrate as mentioned above Or, attaining detailed-ization by changing steeply concentration distribution of the source / drain field of a MOS transistor, and a LDD field near the P-N junction which changes gently inside a field and is formed between substrates The abrupt change of junction leakage current and increment which are generated about the

P-N junction between the impurity range formed in the substrate and a substrate when changing the potential of an impurity or a substrate can be controlled.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Impurity atom concentration profile drawing for the explanation of operation in the 1st example of this invention

[Drawing 2] The process sectional view of the manufacture approach of the semiconductor device in the 2nd example of this invention

[Drawing 3] Impurity atom concentration profile drawing for the explanation of operation in this example

[Drawing 4] The sectional view of the semiconductor device in the 3rd example of this invention

[Drawing 5] The process sectional view of the manufacture approach of the semiconductor device in the 4th example of this invention

[Drawing 6] The sectional view of the semiconductor device in the 5th example of this invention

[Drawing 7] This invention is the process sectional view of the manufacture approach of the semiconductor device in the 6th example.

[Drawing 8] The impurity distribution map for the explanation of operation in the 1st conventional example of this invention

[Drawing 9] The sectional view of the semiconductor device in the 2nd conventional example of this invention

[Description of Notations]

6 Loose Impurity Distribution

7 Steep Impurity Distribution

8 P-N Junction

[Translation done.]

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(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地

(72)発明者　柴田　義行
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(72)発明者　平瀬　順司
大阪府門真市大字門真1006番地　松下電器産業株式会社内

(72)発明者　堀　隆
大阪府門真市大字門真1006番地　松下電器産業株式会社内

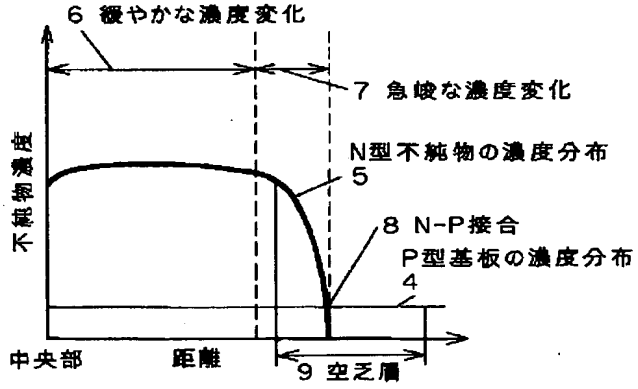
(74)代理人　弁理士　小鍜治　明　（外２名）

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】

【目的】　半導体基板内に形成した基板と反対の導電型の不純物領域について、基板あるいは不純物領域の電位を変化させた場合に、微細化をはかりつつも不純物領域と基板間に形成されるP-N接合リーク電流及びその変化量を低減する。

【構成】　P型基板内のN型不純物領域の不純物濃度分布５状態が、不純物領域内部では緩やかな濃度変化６とし、且つ、P型基板の濃度分布４とN型不純物の濃度分布５間で形成されるN-P接合８近傍では急峻な濃度変化７となるようにすることにより、P-N接合リーク電流及びその変化量を低減することができる、N型の不純物領域を備えた半導体装置である。



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【特許請求の範囲】

【請求項１】一導電型半導体基板内の所定の位置に、前記半導体基板とP-N接合を型成しかつ前記P-N接合付近では濃度分布が急峻に変化し前記P-N接合より離れた領域内部では緩やかな濃度分布である他導電型の不純物領域を備えた半導体装置。

【請求項２】一導電型半導体基板内の所定の位置に、他導電型の不純物をイオン注入で導入し、他導電型の不純物領域を形成する工程と、

フッ素をイオン注入により前記不純物領域の所定の位置に導入する工程と、

前記基板に熱処理を施す工程と、を備えた半導体装置の製造方法。

【請求項３】他導電型の不純物をイオン注入する際に使用した注入マスクをフッ素をイオン注入する時のマスクとして使用することを特徴とする請求項２記載の半導体装置の製造方法。

【請求項４】フッ素のイオン注入を基板に対して大傾角で行なうことを特徴とする請求項２または３に記載の半導体装置の製造方法。

【請求項５】一導電型半導体基板表面に素子分離領域と、

MOS 型トランジスタ領域となる部分に形成されたゲート電極と、

他導電型の不純物からなり、内部では緩やかな濃度分布を持ちながら、基板との間で形成される、所望の位置の接合近傍で濃度分布が急峻に変化するソース・ドレイン領域とを備えた半導体装置。

【請求項６】一導電型半導体基板表面に素子分離領域とMOS型トランジスタ領域となる部分を形成する工程と、

前記MOS型トランジスタ領域となる部分にゲート電極を形成する工程と、

他導電型の不純物をイオン注入で導入し、ソース・ドレイン領域を形成する工程と、

フッ素を前記ソース・ドレイン領域の所定の位置にイオン注入により導入する工程と、

前記基板に熱処理を施す工程と、を備えた半導体装置の製造方法。

【請求項７】ソース・ドレイン領域形成用のイオン注入マスクと、フッ素のイオン注入のマスクとを同一のものを使用することを特徴とする請求項６記載の半導体装置の製造方法。

【請求項８】フッ素のイオン注入を基板に対して大傾角で行なうことを特徴とする請求項６または７に記載の半導体装置の製造方法。

【請求項９】一導電型半導体基板表面に素子分離領域と、

MOS型トランジスタ領域となる部分に形成されたゲート電極と、

前記他導電型の不純物からなるソース／ドレイン領域

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と、

前記ソース／ドレイン領域の全部又は一部を覆う他導電型で前記ソース／ドレイン領域より薄い濃度の不純物領域と、を備えた半導体装置。

【請求項１０】一導電型半導体基板表面に素子分離領域とMOS型トランジスタ領域となる部分を形成する工程と、

前記MOS型トランジスタ領域となる部分にゲート電極を形成する工程と、

他導電型の不純物をイオン注入で導入し、薄い濃度の不純物領域を形成する工程と、

前記他導電型の不純物をイオン注入で導入し、ソース／ドレイン領域を形成する工程と、

フッ素を前記薄い濃度の不純物領域の所定の位置にイオン注入により導入する工程と、

前記基板に熱処理を施す工程と、を備えた半導体装置の製造方法。

【請求項１１】薄い濃度の不純物領域形成用のイオン注入マスクと、フッ素のイオン注入のマスクとを同一のものを使用することを特徴とする請求項１０記載の半導体装置の製造方法。

【請求項１２】フッ素のイオン注入を基板に対して大傾角で行なうことを特徴とする請求項１０または１１に記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、半導体装置及びその製造方法に関するものである。

【０００２】

【従来の技術】従来、半導体基板中への不純物の導入及び不純物領域の形成は、基板を所望の不純物を含む雰囲気中に置き熱処理を行なうといった基板表面からの熱拡散による方法、又、所望の不純物をイオン注入法により基板に導入し不純物の活性化の為の熱処理を加えるといった方法がある。

【０００３】これらの方法を用いた時の基板内での不純物の分布状態を図８を用いて説明する。縦軸は不純物濃度、横軸は距離を示す。まず、熱拡散による導入では、不純物は基板表面から侵入し、かつその不純物はこの熱処理中に拡散していく。この為、不純物の分布１０３は、表面で高濃度になりその後表面から深くなるにつれ、なだらかに減少していく。イオン注入と熱処理を用いた場合、一回のイオン注入について不純物の分布状態はいわゆるガウス分布となり、加速エネルギーにより濃度のピーク位置は決定する。又同一不純物で種々の加速エネルギー、ドーズ量のイオン注入を行なった場合の分布は個々の注入についての分布が重なりあい個々の位置で加算された分布状態となる。

【０００４】ところで、半導体装置ではより一層の微細化を行なうことで、集積度の向上や、性能の向上を図っ

てきている。微細化を行なう手段の１つとして、半導体基板中に導入した導電型不純物の拡散の抑制がある。これは、基板表面に対して水平もしくは垂直方向への不純物の広がりを抑制することで、微細化した個々の素子同士が、物理的に又電気的に短絡することなく動作させることを目的とした方法である。具体的には、熱処理工程の温度を低温化する又は時間を短縮化する方法、例えばMOS型トランジスタのソース／ドレインの様に基板表面付近に不純物領域を形成する場合には不純物の導入を、イオン注入法であればその注入エネルギーを低くするなどして、浅くする方法などである。

【０００５】図９を用いてMOS型構造について説明する。MOS型トランジスタは一般に素子分離１２１、ゲート電極１２２、ソース／ドレイン領域１２８からなる。他に、MOS型トランジスタの構造では、信頼性を確保する為のゲート直下のソース／ドレイン濃度を薄くする例えばLDD(Lightly Doped Drain)領域１２５形成、短チャネル効果抑制の為に基板濃度を基板内の所定の位置のみ濃くする例えばP.T.S.(punch through stop)領域１２６形成、分離耐圧向上の為に素子分離領域直下の基板濃度を濃くする例えばC.S.(channel stop)領域１２４形成などが取り入れられ、性能の向上が図られている。又、これらの不純物領域の形成は上記述べた所望の不純物の熱拡散、又はイオン注入と熱処理の組み合わせにより行なわれている。

【０００６】

【発明が解決しようとする課題】しかしながら上記のような、熱拡散やイオン注入と熱処理の組み合わせで不純物領域を形成する方法では、図８を用いて説明すると、不純物の分布状態は、領域内部で高濃度のピーク位置を持ち、そのすぐ前後の位置から濃度の分布は急峻となってしまう、つまり浅いが急峻な分布１０４となるか、あるいは領域内部の分布状態が緩やかであっても不純物がかなり拡散して水平／垂直両方向に広がってしまう、つまり緩やかだが深い分布１０５になってしまう。

【０００７】この時、不純物領域と基板との間でP-N接合１１１が形成されるが、不純物の分布状態が不純物領域内部で高濃度のピークを持ち、このピーク位置からテール位置まで急峻な分布である場合、不純物領域の電位が変化し、これに伴い空乏層幅が変化すると不純物領域の濃度分布が急峻な為に接合リーク電流の変化量も急激になってしまい基板電位も大きく変化してしまうといった問題が生じてくる。又、不純物の濃度も高くなるため接合リーク電流そのものも増加してしまい回路を構成した際の消費電力が増加してしまうといった問題が生じてくる。

【０００８】又、形成工程を簡略的にした場合では、不純物領域内部の分布状態が緩やかにする為にはイオン注入で導入した不純物を熱処理により十分に拡散させる必要がある。この場合は不純物領域が広がることから微細

化をはかることが困難になるといった問題が生じてくる。

【０００９】他に不純物領域内部の分布を緩やかにし、且つ不純物領域を水平及び垂直方向に拡散させない方法には例えば図８(b)に示す方法がある。即ち、不純物導入のイオン注入を加速エネルギーを段階的に変えて多数回１０６行ない、活性化の熱処理を低温でかつ短時間行なう。この方法では前記の様な問題を生じる分布状態にならない。しかしながらこの方法では、不純物導入の為のイオン注入を、加速エネルギーを変えて多数回実施する必要があり、工程増加によるコストの増加が生じてしまうといった問題がある。

【００１０】従って、本発明の目的は、不純物領域を基板内水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成した不純物領域と基板間の P-N 接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制する半導体装置、及びその製造方法を提供することにある。

【００１１】

【課題を解決するための手段】請求項１記載の半導体装置は上記問題点に鑑み、不純物領域を基板内水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成した不純物領域と基板間のP-N接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制する半導体装置を提供するものである。この為の構成として、一導電型半導体基板内の所定の位置に、前記半導体基板とP-N接合を形成しかつ前記P-N接合付近では濃度分布が急峻に変化し前記P-N接合より離れた領域では緩やかな濃度分布である他導電型の不純物領域を有する構造を特徴とする。

【００１２】請求項２、３、４記載の半導体装置の製造方法は上記問題点に鑑み、不純物領域を基板内水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成した不純物領域と基板間のP-N接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制する半導体装置の製造方法を提供するものである。この為の構成として、一導電型半導体基板内の所定の位置に、他導電型の不純物をイオン注入で導入し、前記他導電型の不純物領域を形成する工程と、フッ素をイオン注入により前記不純物領域の所定の位置に導入する工程と、前記基板に熱処理を施す工程とを有することを特徴とする。

【００１３】請求項５記載の半導体装置は上記問題点に鑑み、MOS型トランジスタのソース／ドレイン領域を、基板内水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成したソース／ドレイン領域と基板間のP-N接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制する半導体装置を提供するものである。この為の構成として、一導電型半導体基板表面に素子分離領域と、MO

S型トランジスタ領域となる部分に形成されたゲート電極と、他導電型の不純物からなり、内部では緩やかな濃度分布を持ちながら、所望の位置の、基板との間で形成される接合近傍で濃度分布が急峻に変化するソース・ドレイン領域とを有することを特徴とする。

【００１４】請求項６、７、８記載の半導体装置の製造方法は上記問題点に鑑み、MOS型トランジスタのソース／ドレイン領域を、基板内水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成したソース／ドレイン領域と基板間のP-N接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制する半導体装置の製造方法を提供するものである。この為の構成として、一導電型半導体基板表面に素子分離領域とMOS型トランジスタ領域となる部分を形成する工程と、前記MOS 型トランジスタ領域となる部分にゲート絶縁膜を形成する工程と、他導電型の不純物をイオン注入で導入し、ソース・ドレイン領域を形成する工程と、レジストをマスクとしてフッ素を前記ソース・ドレイン領域の所定の位置にイオン注入により導入する工程と、前記基板に熱処理を施す工程とを有することを特徴とする。

【００１５】請求項９記載の半導体装置は上記問題点に鑑み、MOS型トランジスタのLDD領域を、基板内水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成したソース／ドレイン領域と基板間のP-N接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制する半導体装置を提供するものである。この為の構成として、一導電型半導体基板表面に素子分離領域と、MOS型トランジスタ領域となる部分に形成されたゲート電極と、前記半導体基板と他方導電型のLDD領域と、他導電型の不純物からなるソース／ドレイン領域とを有することを特徴とする。

【００１６】請求項１０、１１、１２記載の半導体装置の製造方法は上記問題点に鑑み、MOS型トランジスタのLDD領域を、基板内水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成したソース／ドレイン領域と基板間のP-N接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制する半導体装置の製造方法を提供するものである。この為の構成として、一導電型半導体基板表面に素子分離領域とMOS型トランジスタ領域となる部分を形成する工程と、前記MOS 型トランジスタ領域となる部分にゲート絶縁膜を形成する工程と、他導電型の不純物をイオン注入で導入し、LDD領域を形成する工程と、前記他導電型の不純物をイオン注入で導入し、ソース／ドレイン領域を形成する工程と、フッ素を前記比較的薄い不純物濃度である領域の所定の位置にイオン注入により導入する工程と、前記基板に熱処理を施す工程とを有することを特徴とする。

【００１７】

【作用】請求項１、５及び９に係る半導体装置により、基板内に形成した不純物領域あるいは、MOS型トランジスタのソース／ドレイン領域及びLDD領域を水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成した不純物領域と基板間のP-N 接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制することが可能となる。

【００１８】請求項２、３、４、６、７、８、１０、１１、１２に係る半導体装置の製造方法により、基板内に形成した不純物領域あるいは、MOS型トランジスタのソース／ドレイン領域及びLDD領域を水平及び垂直方向で広げず、微細化を図ったままで、基板内に形成した不純物領域と基板間のP-N接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制することが可能となる。

【００１９】

【実施例】以下請求項１記載の半導体装置の一実施例として、P型基板内に形成されたN型不純物領域の場合、微細化を図りつつも、基板と不純物領域間で形成されるP-N接合のリーク電流及びその変化量を低減できる装置について図面を参照しながら説明する。

【００２０】図１は本発明の実施例における動作説明の為の不純物濃度分布図である。図１では、P型基板内に形成されたN型不純物の濃度について横軸を距離、縦軸を不純物濃度、横軸の原点を不純物領域の中央部とした際、P型基板の不純物分布４、N型不純物の濃度分布５、又、N型不純物の濃度分布５の中で緩やかな濃度変化６の領域と急峻な濃度変化７の領域及び、N型不純物領域とP型基板間で形成されるN-P接合８を示している。但し、この際N-P接合８はN型不純物領域について急峻な濃度変化７に位置するものとする。

【００２１】一般に、P-N接合のP型もしくはN型領域の何れかの電位を変化させるとP-N接合で形成される空乏層幅が変化し接合電流が流れる。本構成をとることにより、例えばN型不純物領域の電位が正方向に変化するとN-P接合の空乏層幅９が広がるが、空乏層領域が緩やかな濃度変化６領域に達した場合には、ここで濃度変化が緩やかになることにより、接合リーク電流の増加量も低減できる。この為接合部からのリーク電流の絶対値自体も低減でき、例えば、回路を形成した場合の消費電力も低減できる。

【００２２】又、接合部近傍の濃度変化は急峻であるため、不純物領域を広げることなく素子の微細化を図ることも可能である。

【００２３】以上の様に、本実施例によれば、素子の微細化を図りつつも基板と不純物領域の接合部で生じるリーク電流及びその変化量の増加を抑制することができる。

【００２４】以下請求項２、３及び４記載の半導体装置

の製造方法の１実施例としてP型基板に、N型不純物領域を形成した際に、微細化を図りつつも、基板と不純物領域間で形成されるP-N接合のリーク電流及びその変化量を低減できる製造方法について図面を参照しながら説明する。

【００２５】図２は本発明の実施例の工程断面図である。又図３は、同実施例における動作説明のための不純物濃度分布図である。

【００２６】図２(a) ではP型シリコン基板２１にイオン注入マスク２２を用いて、例えばP, 30KeV, 5E15atoms/cm2といった条件でN型不純物のイオン注入２３を行ない、N型不純物領域２４を形成する。

【００２７】図２(b)では、注入マスク２５を用いてフッ素のイオン注入２６を例えば35KeV, 2E15atoms/cm2といった条件で行ない、N型不純物領域２４の底部に、(F)フッ素領域２７を形成する。その後基板２１に熱処理を行ないN型不純物の活性化を行なう。

【００２８】図３では、上記の熱処理を行なった際のN型不純物及びFの濃度分布を示している。縦軸は不純物濃度、横軸は距離を表す。図３(a)ではP型基板にN型不純物をイオン注入により導入した直後の濃度分布２９に対してFの濃度分布のピーク位置３０がN型不純物の濃度分布のピーク位置３２を越える様なイオン注入直後のFの濃度分布３１を設定する。この分布状態で熱処理を施す。

【００２９】図３(b)では、熱処理後、N型不純物の濃度分布３３は、従来のフッ素注入を行なわない場合の熱処理後の分布３４に比べて、フッ素 (F)の拡散抑制効果の影響によりN型不純物領域の内部では緩やかな変化をもつが、ピークより離れた位置で急峻に変化する。

【００３０】この時、不純物領域の熱処理中での拡散が抑制されるので素子の微細化が図れる。加えてN型不純物の分布状態が領域内部では緩やかに変化するが、基板とのP-N接合付近では急峻に変化するので例えば、不純物領域の電位が変化して接合部の空乏層幅が広がった場合でも緩やかなN型の不純物分布状態の為、接合部のリーク電流が増加することなく又その変化量も緩やかであるため基板電位自体も大きく変化することがない。その為、安定した良好な半導体素子が形成できる。

【００３１】なお、図２(b)に示す工程の代わりに図２(c)に示すように、N型の不純物のイオン注入用マスク２２を使用してフッ素注入を行なっても良く、工程の簡略化が図れる。この時、フッ素注入を大傾角θでおこなうことによりN型不純物領域２４に対して底部のみならず任意の位置にフッ素の領域２８を形成できる。

【００３２】以上の様に、本実施例によれば、素子の微細化を図りつつも基板と不純物領域の接合部で生じるリーク電流及びその変化量の増加を抑制することができる。

【００３３】以下請求項５記載の半導体装置の１実施例としてP型基板に形成したMOS型トランジスタについて、微細化を図りつつも、基板と不純物領域間で形成されるP-N接合のリーク電流及びその変化量を低減できる装置について図面を参照しながら説明する。図４は本発明をMOS型トランジスタに適用した場合の半導体装置の断面図である。

【００３４】図４(a) では、ゲート電極４１、素子分離４９、ソース／ドレイン用N型不純物領域４５からなるMOS型トランジスタにおいて、ソース／ドレイン用N型不純物領域４５の濃度分布状態を、領域内部では緩やかな濃度変化領域４２とし、領域底部と基板との接合近傍では急激な濃度変化領域４３とする。

【００３５】本構成をとることにより、ソース／ドレイン用N型不純物領域４５の電位が例えば正方向に変化するとN-P接合４４の空乏層幅が広がるが、空乏層領域が緩やかな濃度変化４３領域に達した場合には、ここで濃度変化が緩やかになることにより、接合リーク電流の増加量も低減できる。その変化量が緩やかであるため基板電位が大きく変化することがない。又、接合部からのリーク電流の絶対値自体も低減でき、例えば、回路を形成した場合の消費電力も低減できる。さらに接合部近傍の濃度変化は急峻であるため、例えば素子の微細化を図ることも可能である。

【００３６】図４(b)では、MOS型トランジスタのソース／ドレイン用N型不純物領域４５についてゲート電極直下側および素子分離直下側の不純物分布を急激な濃度変化領域２(43b)、及び急激な濃度変化領域１(43a)とすることにより、トランジスタの基本特性である単チャネル効果を抑制または分離特性を向上させ、微細化を図るとともに接合リーク電流及びその変化量の増加を低減できる。

【００３７】以上の様に、本実施例によれば、素子の微細化を図りつつも基板と不純物領域の接合部で生じるリーク電流及びその変化量の増加を抑制することができる。

【００３８】以下請求項６、７及び８記載の半導体装置の製造方法１実施例としてP型基板にMOS型トランジスタを形成する場合について、微細化を図りつつも、基板と不純物領域間で形成されるP-N接合のリーク電流及びその変化量を低減できる製造方法について図面を参照しながら説明する。図５は本発明をMOS型トランジスタの製造方法に適用した場合の工程断面図である。

【００３９】図５(a)では、P型基板２１にゲート電極４１、素子分離４９からなるMOS型トランジスタを形成するにあたり、注入マスク２２を用いてイオン注入によりソース／ドレイン用N型不純物５１を導入し、ソース／ドレイン用N型不純物領域４５を形成する。

【００４０】図５(b)では、注入マスク２５を用いてイオン注入によりフッ素(F)を導入し、ソース／ドレイン用 N型不純物領域４５の底部にフッ素(F)領域５３を形

成する。その後基板２１に熱処理を加える。

【００４１】図５(c)では、上記工程を行なうことによりソース／ドレイン用 N型不純物領域４５の濃度分布状態を、領域内部では緩やかな濃度変化領域５４とし、領域底部と基板との接合近傍では急激な濃度変化領域５６とする。

【００４２】本構成をとることにより、ソース／ドレイン用N型不純物領域４５の電位が例えば正方向に変化するとN-P接合５６の空乏層幅が広がるが、空乏層領域が緩やかな濃度変化５４領域に達した場合には、ここで濃度変化が緩やかになることにより、接合リーク電流の増加量も低減できる。その変化量が緩やかであるため基板電位が大きく変化することがない。又、接合部からのリーク電流の絶対値自体も低減でき、例えば、回路を形成した場合の消費電力も低減できる。さらに接合部近傍の濃度変化は急峻であるため、例えば素子の微細化を図ることも可能である。

【００４３】なお、図５(c)に示す工程の代わりに図５(d)に示すように、N型の不純物のイオン注入用マスク２２を使用してフッ素注入を行なっても良く、工程の簡略化が図れる。この時、フッ素注入を大傾角θでおこなうことによりN型不純物領域４５に対して底部のみならず例えばゲート電極直下側や素子分離直下側の領域といった任意の位置にフッ素の領域５８を形成できる。これにより工程を増やすことなくトランジスタの基本特性である単チャネル効果を抑制または分離特性を向上させ、微細化を図るとともに接合リーク電流及びその変化量の増加を低減できる。

【００４４】以上の様に、本実施例によれば、素子の微細化を図りつつも基板と不純物領域の接合部で生じるリーク電流及びその変化量の増加を抑制することができる。

【００４５】以下請求項９記載の半導体装置の１実施例として、P型基板に形成したMOS型トランジスタについて、微細化を図りつつも、基板と不純物領域間で形成されるP-N接合のリーク電流及びその変化量を低減できる装置について図面を参照しながら説明する。図６は本発明をＬＤＤ構造を有するMOS型トランジスタに適用した場合の、半導体装置の断面図である。

【００４６】図６では、ゲート電極４１、素子分離４９、LDD領域８１、ソース／ドレイン用N型不純物領域８２からなるMOS型トランジスタにおいて、LDD領域８１の濃度分布状態を、領域内部では緩やかな濃度変化領域８３とし、領域と基板との接合近傍では急激な濃度変化領域８４とする。

【００４７】本構成をとることにより、LDD領域８１の電位が例えば正方向に変化するとN-P接合の空乏層幅が広がるが、空乏層領域が緩やかな濃度変化８３領域に達した場合には、ここで濃度変化が緩やかになることにより、接合リーク電流の増加量も低減できる。その変化量が緩やかであるため基板電位が大きく変化することがない。又、接合部からのリーク電流の絶対値自体も低減でき、例えば、回路を形成した場合の消費電力も低減できる。さらに接合部近傍の濃度変化は急峻であるため、例えば素子の微細化を図ることも可能である。

【００４８】以上の様に、本実施例によれば、素子の微細化を図りつつも基板と不純物領域の接合部で生じるリーク電流及びその変化量の増加を抑制することができる。

【００４９】以下請求項１０、１１及び１２記載の半導体装置の製造方法の１実施例として、P型基板にMOS型トランジスタを形成する場合について、微細化を図りつつも、基板と不純物領域間で形成されるP-N接合のリーク電流及びその変化量を低減できる製造方法について図面を参照しながら説明する。図７は本発明をＬＤＤ構造を有するMOS型トランジスタの製造方法に適用した場合の、工程断面図である。

【００５０】図７(a)では、P型基板２１にゲート電極４１、素子分離４９からなるMOS型トランジスタを形成するにあたり、注入マスク６３を用いてイオン注入によりLDD用N型不純物61を導入し、LDD用 N型不純物領域６２を形成する。

【００５１】図７(b)では、注入マスク２５を用いてイオン注入によりフッ素(F)を導入し、LDD用N型不純物領域６２の底部にフッ素(F)領域５３を形成する。その後基板２１に熱処理を加える。

【００５２】図７(c)では、ゲート電極４１に対してサイドウォール６４を形成し、その後ゲート電極と注入マスク２２をマスクとしてイオン注入によりソース／ドレイン用の濃いN型不純物の導入６８を行ない、LDD用N型不純物領域６２内の一部もしくは全部と重なるようにソース／ドレイン領域６５を形成する。その後基板２１に熱処理を加える。

【００５３】本構成をとることにより、LDD用N型不純物領域６２の電位が例えば正方向に変化するとN-P接合の空乏層幅が広がるが、空乏層領域が緩やかな濃度変化領域に達した場合には、ここで濃度変化が緩やかになることにより、接合リーク電流の増加量も低減できる。その変化量が緩やかであるため基板電位が大きく変化することがない。又、接合部からのリーク電流の絶対値自体も低減でき、例えば、回路を形成した場合の消費電力も低減できる。さらに接合部近傍の濃度変化は急峻であるため、例えば素子の微細化を図ることも可能である。

【００５４】なお図７(c)に示す工程の代わりに図７(d)に示す、LDD用の薄いN型の不純物のイオン注入用マスク２２を使用してフッ素注入を行なっても良く、工程の簡略化が図れる。又、この時、フッ素注入６６を大傾角θでおこなうことによりLDD用N型不純物領域６２に対して底部のみならず例えばゲート電極直下側や素子分離直下側の領域といった任意の位置にフッ素の領域６７を形成

できる。これにより工程を増やすことなくトランジスタの基本特性である単チャネル効果を抑制または分離特性を向上させ、微細化を図るとともに接合リーク電流及びその変化量の増加を低減できる。

【００５５】以上の様に、本実施例によれば、素子の微細化を図りつつも基板と不純物領域の接合部で生じるリーク電流及びその変化量の増加を抑制することができる。

【００５６】尚、上記実施例においてN型基板にP型の不純物領域やソース／ドレイン領域、LDD領域を形成した場合においても同様な効果が得られる。

【００５７】

【発明の効果】以上のように本発明は、基板内に形成した不純物領域あるいは、MOS型トランジスタのソース／ドレイン領域及びLDD領域の濃度分布を、領域内部では緩やかに変化し、且つ基板との間で形成されるP-N接合近傍では急峻に変化させることにより、微細化を図ったままで、基板内に形成した不純物領域と基板間のP-N接合について、不純物又は基板の電位を変化させた時に発生する接合リーク電流の急激な変化及び増加を抑制することができる。

【図面の簡単な説明】

【図１】本発明の第１の実施例における動作説明の為の不純物濃度分布図

【図２】本発明の第２の実施例における半導体装置の製造方法の工程断面図

【図３】同実施例における動作説明のための不純物濃度分布図

【図４】本発明の第３の実施例における半導体装置の断面図

【図５】本発明の第４の実施例における半導体装置の製造方法の工程断面図

【図６】本発明の第５の実施例における半導体装置の断面図

【図７】本発明は第６の実施例における半導体装置の製造方法の工程断面図

【図８】本発明の第１の従来例における動作説明の為の不純物分布図

【図９】本発明の第２の従来例における半導体装置の断面図

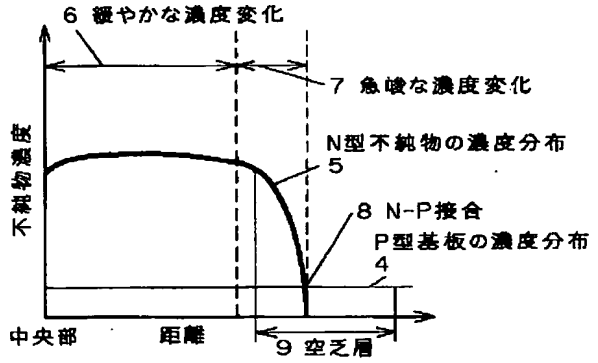
【符号の説明】

6　緩やかな不純物分布

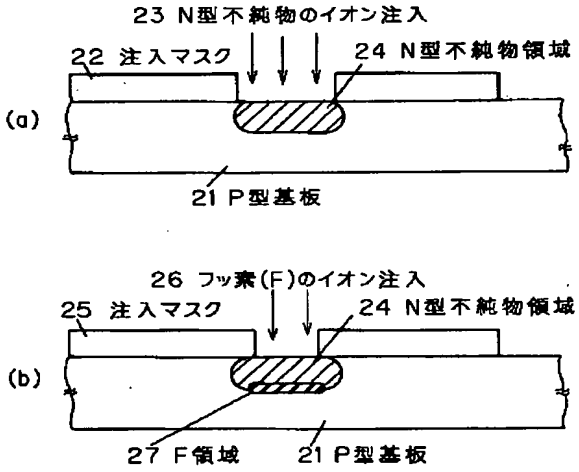
7　急峻な不純物分布

8　P-N接合

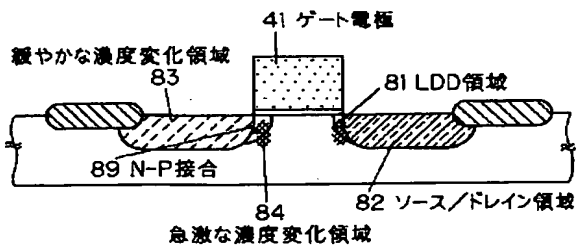
【図１】



【図２】

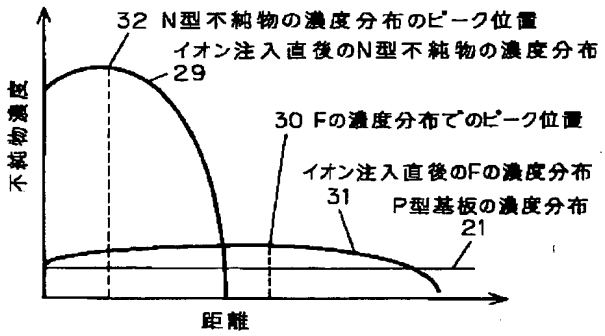


【図６】



【図３】

(a)



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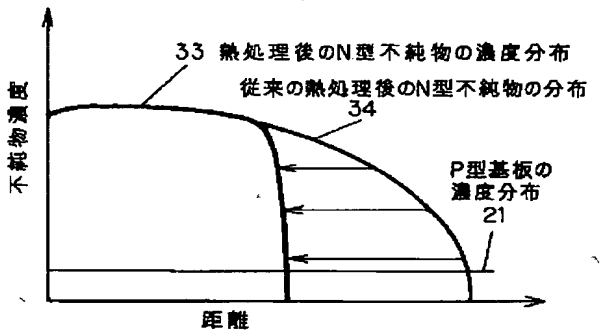
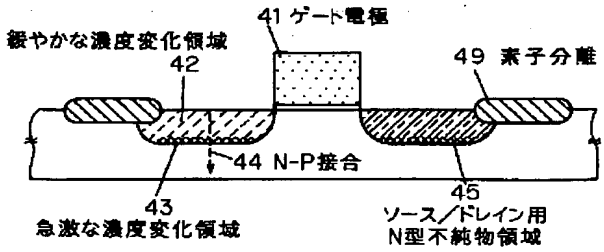


【図４】

(a)



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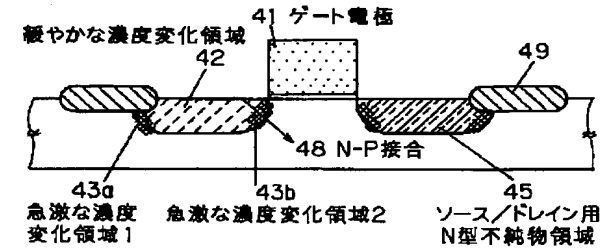
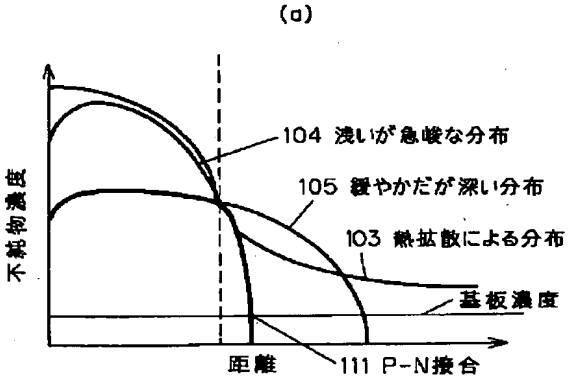


【図８】

(a)



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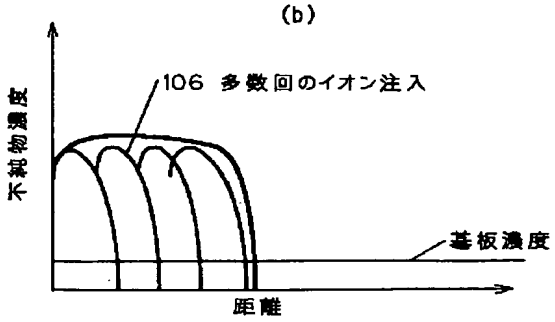
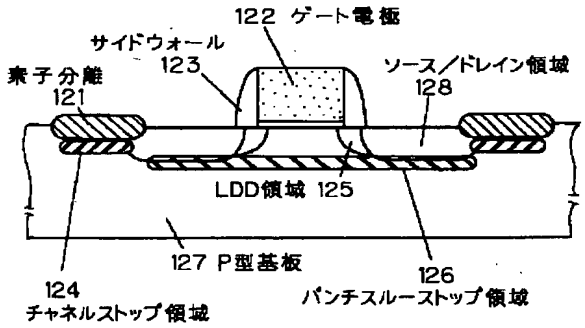
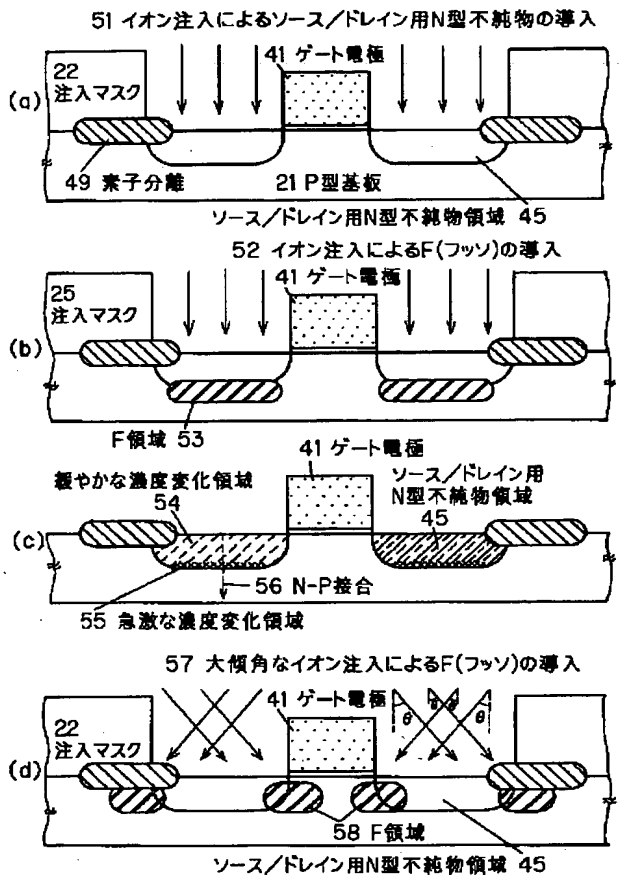


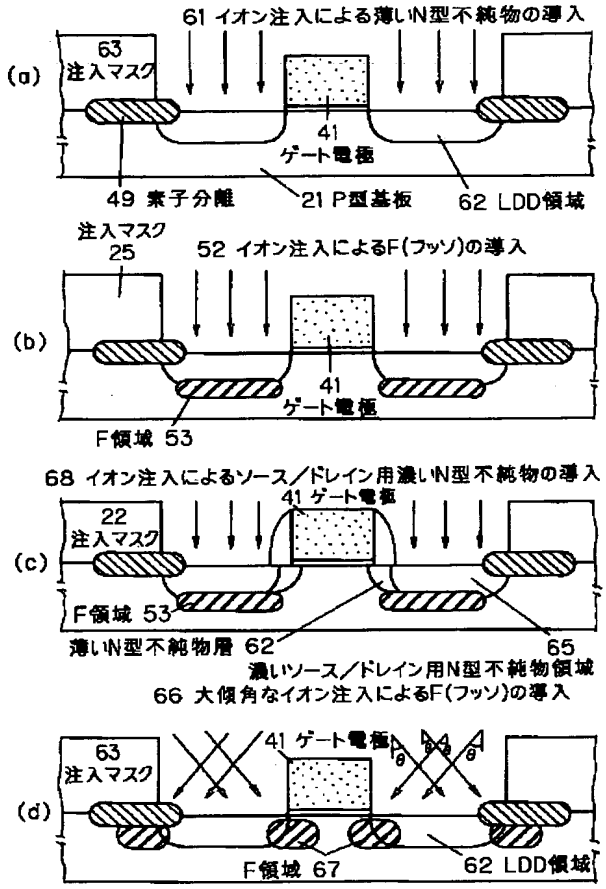
【図９】



【図５】


51 イオン注入によるソース/ドレイン用N型不純物の導入
22
注入マスク
41 ゲート電極
(a)
49 素子分離
21 P型基板
ソース/ドレイン用N型不純物領域 45
52 イオン注入によるF(フッソ)の導入
25
注入マスク
41 ゲート電極
(b)
F領域 53
41 ゲート電極
緩やかな濃度変化領域
54
ソース/ドレイン用
N型不純物領域
45
(c)
56 N-P接合
55 急激な濃度変化領域
57 大傾角なイオン注入によるF(フッソ)の導入
22
注入マスク
41 ゲート電極
θ
(d)
58 F領域
ソース/ドレイン用N型不純物領域 45

【図７】


61 イオン注入による薄いN型不純物の導入
63
注入マスク
(a)
41
ゲート電極
49 素子分離
21 P型基板
62 LDD領域
注入マスク
25
52 イオン注入によるF(フッソ)の導入
(b)
41
ゲート電極
F領域 53
68 イオン注入によるソース/ドレイン用濃いN型不純物の導入
41 ゲート電極
22
注入マスク
(c)
F領域 53
薄いN型不純物層 62
65
濃いソース/ドレイン用N型不純物領域
66 大傾角なイオン注入によるF(フッソ)の導入
63
注入マスク
41 ゲート電極
θ
(d)
F領域 67
62 LDD領域